CLAIMS

- 1 1. (Original) A system for facilitating inter-processor communication in a
- 2 multiple processor computer system having one or more shared resources, comprising:
- a first mailbox associated with a first processor for indicating the status of the
- 4 shared resources in the system and for sharing one or more tasks among the multiple-
- 5 processors;
- a second mailbox associated with a second processor for indicating the status of
- 7 the shared resources in the system and for sharing one or more tasks among the multiple
- 8 processors; and
- a semaphore unit for indicating the status of the shared resources in the system
- and for notifying the first and second processors of a particular task to be executed by
- 11 the respective processors.
- 1 2. (Original) The system of Claim 1, wherein the first processor is a host
- 2 processor and the second processor is a co-processor.
- 1 3. (Original) The system of Claim 1, wherein the tasks are shared among the
- 2 multiple processors without latency.
- 4. (Original) The system of Claim 1, wherein either the first or second mailbox
- 2 receives a message from the semaphore unit indicating a task to be executed, and
- 3 wherein the first or second mailbox notifies its associated processor of the message.

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- 1 5. (Original) The system of Claim 4, wherein either the first or second mailbox
- 2 causes a respective interrupt signal to be communicated to its associated processor when
- a message is received from the semaphore unit.
- 6. (Original) The system of Claim 5, wherein, in response to the respective
- 2 interrupt signal, the associated processor services the interrupt signal by reading the
- 3 message from the associated mailbox.
- 1 7. (Original) The system of Claim 6, wherein upon reading the message from the
- associated mailbox, the mailbox is cleared and an acknowledge notification is
- 3 communicated by the mailbox to the other processor to indicate that the mailbox is
- 4 empty and that the task is being executed.
- 1 8. (Original) The system of Claim 1, wherein the semaphore unit comprises a first
- 2 plurality of semaphore registers for indicating the status of a shared resource in the
- 3 system and a second plurality of semaphore registers for indicating messages that are
- 4 communicated to the first and second mailboxes to notify a respective processor of a
- 5 task to be executed.
- 9. (Original) The system of Claim 8, wherein the semaphore registers are
- 2 controlled by a semaphore controller.
- 1 10. (Original) The system of Claim 8, wherein the first plurality of semaphore

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- 2 registers comprises a first register for indicating the status of a shared resource in the
- system, a second register for setting particular bits in the first register to indicate the
- 4 data stored in a particular memory location of the shared resource, and a third register
- 5 for clearing particular bits in the first register.
- 1 11. (Original) The system of Claim 10, wherein the first, second, and third registers
- 2 are 32 bit registers.
- 1 12. (Original) The system of Claim 10, wherein the first register comprises a first bit
- 2 portion wherein each individual bit is associated with a particular shared resource in the
- 3 · system, and a second bit portion for indicating the data stored in a particular memory
- 4 location of that particular shared resource.
- 1 13. (Original) The system of Claim 12, wherein the first bit portion comprises six
- 2 bits such that the most significant bit in the first bit portion is associated with a host
- 3 instruction memory, the next most significant bit in the first bit portion is associated
- 4 with a ping buffer, the next most significant bit in the first bit portion is associated with
- 5 a pong buffer, the next most significant bit in the first bit portion is associated with a
- 6 coprocessor instruction memory, the next most significant bit in the first bit portion is
- 7 associated with a cache memory, and the least significant bit in the first bit portion is
- 8 associated with input/output resources.
- 1 14. (Original) The system of Claim 12, wherein in response to being notified of a

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- 2 task to be executed, the respective processor reads the data from the first register to
- 3 execute the task.
- 1 15. (Original) The system of Claim 8, wherein the second plurality of registers
- 2 comprises a fourth register and a fifth register each for indicating a message for the
- 3 respective mailboxes of a task to be executed.
- 1 16. (Currently Amended) A system for facilitating inter-processor communication in
- 2 a multiple processor computer system having one or more shared resources, comprising:
- means for cooperatively multitasking and preemptively multitasking among the
- 4 multiple processors;
- 5 <u>semaphore means for preemptively multitasking;</u>
- means for notifying a respective processor of a particular task to be executed;
- 7 means for indicating the status of the shared resources in the system; and
- 8 means for communicating the status of a particular shared resource to the
- 9 processor for execution of the task.
- 1 17. (Original) A method for facilitating inter-processor communication in a multiple
- 2 processor computer system having one or more shared resources, comprising the steps
- 3 of:
- 4 sending a message to a first mailbox indicating a task to be executed by a first
- 5 processor;
- 6 notifying the first processor of the message;

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- 7 reading the message from the first mailbox;
- 8 configuring a first semaphore register to indicate the data contained at a desired
- 9 address location of a particular one of the shared resources; and
- accessing the first semaphore register and reading the data from the first
- semaphore register to execute the task.
- 1 18. (Original) The method of Claim 17, wherein the notifying step comprises the
- 2 step of interrupting the first processor with an interrupt signal.

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- 4 19. (Original) The method of Claim 17, wherein upon performing the reading step
- 5 further performing the step of clearing the message from the first mailbox and sending
- 6 an acknowledge message to a second processor informing the second processor that the

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- 7 first mailbox is empty and that the task is being performed.
- 1 20. (Original) The method of Claim 17, further comprising the step of
- 2 clearing the data in the first semaphore register.

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